Refine Search

Search Results -

Terms	Documents
L1 same (switch same (chip or (integrated adj1 circuit) or IC))	124

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, July 28, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L3	L1 same (switch same (chip or (integrated adj1 circuit) or IC))	124	L3
L2	L1 and (switch same (chip or (integrated adj1 circuit) or IC))	197	L2
L1	processor same memory same crossbar	704	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L3	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Wednesday, July 28, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=USPT,USOC; PLUR=YES; OP=OR			
L3	L1 same (switch same (chip or (integrated adj1 circuit) or IC))	124	L3
L2	L1 and (switch same (chip or (integrated adj1 circuit) or IC))	197	L2
L1	processor same memory same crossbar	704	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
(358/444 |358/462 |716/1 |709/213 |709/249 |340/2.28 |710/317 |710/100 |710/316 |370/381 |370/351 |370/362 |703/1 |712/11 |712/20 |712/35 |382/276).ccls.	6306

Database:
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- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L5

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, July 28, 2004 Printable Copy Create Case

Set Name side by side	Query
	DB=USPT,USOC; PLUR=YES; OP=OR
L5	710/317,100,316;703/1;716/1;370/381,351,362;709/213,249;712/11,20,35;340/2.28;382/276;358/
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR
L4	L3
	DB=USPT,USOC; PLUR=YES; OP=OR
L3	L1 same (switch same (chip or (integrated adj1 circuit) or IC))
L2	L1 and (switch same (chip or (integrated adj1 circuit) or IC))
L1	processor same memory same crossbar

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L3 and L5	45

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L6

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, July 28, 2004 Printable Copy Create Case

Set Name side by side	Query
	DB=USPT,USOC; PLUR=YES; OP=OR
L6	l3 and L5
L5	710/317,100,316;703/1;716/1;370/381,351,362;709/213,249;712/11,20,35;340/2.28;382/276;358/
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR
L4	L3
	DB=USPT,USOC; PLUR=YES; OP=OR
L3	L1 same (switch same (chip or (integrated adj1 circuit) or IC))
L2	L1 and (switch same (chip or (integrated adj1 circuit) or IC))
L1	processor same memory same crossbar

END OF SEARCH HISTORY

h e b b cg b e e ch

L7: Entry 2 of 15 File: USPT May 30, 2000

DOCUMENT-IDENTIFIER: US 6070003 A
TITLE: System and method of memory access in apparatus having plural processors and plural memories

Abstract Text (1):
There is disclosed a multi-processor system and method arranged, in one embodiment, as an image and graphics processor. The image processor is structured with several individual processors all having communication links to several memories. A crossbar switch serves to establish the processor memory links. The entire image processor, including the individual processors, the crossbar switch and the memories, is contained on a single silicon chip.

Brief Summary Text (19):
The problems inherent with constructing a single chip image processor having a high degree of versatility have been solved by the architecture of establishing a multi-link, multi-bus crossbar switch between the individual processors and the individual memories. This architecture, coupled with the design of the high density switch, allows the system to perform in both the SIMD and MIMD modes and allows for access of all processors to all memories. The crossbar switch is constructed with different length links serving different functions so as to conserve space while still providing a high degree of operational flexibility.

Detailed Description Text (11):
Crossbar switch 20 is shown distributed, and in this form tends to mitigate communication bottlenecks so that communications can flow easily between the various parts of the system. The crossbar switch is integrated on a single chip with the processors and with the memory thereby further enhancing communications among the system elements.

Detailed Description Text (134):
One of the reasons why so much imaging capability is available under the system shown is that the single chip contains several processors working in parallel together with several memories, all accessible under a crossbar switch which allows for substantially instantaneous rearrangement of the system. This gives a degree of power and flexibility not heretofore known. This then allows for a vast increase in the amount of imaging processing capability which can be utilized in conjunction with other processing capability to provide the type of services not known before. Some examples of this would be restoration of photographs and other images, or the cleaning of facsimile documents so that extraneous material in the background is removed yielding a received image as clear or clearer than the sending image. This entire system can be packaged in a relatively small package mainly because of the processing capability that is combined into one operational unit. Bandwidth limitations and other physical limitations such as wiring connections, are eliminated.

Current US Original Classification (1):
710/317

h e b b cg b cc e

L7: Entry 2 of 15 File: USPT May 30, 2000

US-PAT-NO: 6070003
DOCUMENT-IDENTIFIER: US 6070003 A

TITLE: System and method of memory access in apparatus having plural processors and plural memories

DATE-ISSUED: May 30, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gove; Robert J.	Plano	TX		
Balmer; Keith	Bedford			GB
Ing-Simmons; Nicholas Kerin	Bedford			GB
Guttag; Karl Marion	Missouri City	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 08/ 264582 [PALM]
DATE FILED: June 22, 1994

PARENT-CASE:
This application is a Continuation of application Ser. No. 07/437,852, filed Nov. 17, 1989 abandoned.

INT-CL: [07] G06 F 13/16

US-CL-ISSUED: 395/312
US-CL-CURRENT: 710/317

FIELD-OF-SEARCH: 395/200, 395/800

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4365292	December 1982	Barnes et al.	395/800
☐	4553203	November 1985	Rau et al.	395/800
☐	4562535	December 1985	Vincent et al.	364/200

☐	4633245	December 1986	Blout et al.	340/825.03
☐	4644496	February 1987	Andrews	364/900
☐	4747043	May 1988	Rodman	364/200
☐	4807184	February 1989	Shelor	364/900
☐	4811201	March 1989	Rau et al.	395/325
☐	4930102	May 1990	Jennings	395/800
☐	4965718	October 1990	George et al.	395/800
☐	4985832	January 1991	Grondalski	395/800
☐	5020059	May 1991	Gonin et al.	395/800
☐	5041971	August 1991	Carvey et al.	395/800
☐	5056000	October 1991	Chang	395/800
☐	5083267	January 1992	Rau et al.	395/375
☐	5133073	July 1992	Jackson et al.	395/800
☐	5142686	August 1992	Hecht et al.	395/800

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 245 996	November 1987	EP	
WO 88/08167	October 1988	WO	

OTHER PUBLICATIONS

A. M. Despain, et al., "High Performance Prolog, The Multiplicative Effect of Several Levels of Implementation", IEEE, pp. 178-184, 1986.
"VITec Parallel C Compiler", by T. Butler, published by Visual Information Technologies, Inc. Plano TX, pp. 741-747.
"A Single Board image computer with 64 Parallel Processors", by Stephen Wilson, published in Electronic Imaging '87, International Electronic Imaging Exposition & Conference, (1987) pp. 470-475.
"The Androx Parallel Image Array Processor", by Wayne Threatt, in Electronic Imaging '87, International Electronic Imagining Exposition & Conference (1987), pp. 1061-1064.
"Real Time 3D Object Tracking in a Rapid Prototyping Environment", by Robert J. Gove in Electronic Imaging '88 (1988).
"Integration of Symbolic and Multiple Digital Signal Processors with the Explorer/Odyssey for Image Processing and Understanding Applications", by Robert J. Gove, in Proceeding of the IEEE International Symposium on Circuits and Systems, pp. 968-971 (May, 1987).
"The Use of Parallel-Processing Computers in Digital Image Processing", by Lew Brown, published by Alliant Computer Systems Corp., Litteton, MA.
"The Connection Machine", by W.D. Hillis, published in The MIT Press (1985).
"Handling Real Time Images Comes Naturally to Systolic Array Chip", by Hannaway, Shea Bishop, in Electronic Design, p. 289-300 (1984).
"Systolic Array Chip Recognizes Visual Patterns Quicker Than a Wink", by W.W. Smith, P. Sullivan, in Electronic Design, pp. 257-266 (1984).
"Design of a Massively Parallel Processor", by Kenneth Batcher, IEEE Transactions on Computers, v. C-29, No. 9 (1980).
"High Resolution Frame Grabbing and Processing Through Parallel Architecture", by

Daniel Crevier published by Coreco, Inc., Quebec, Canada.
Multiple Digital Signal Processor Environment for Intelligent Signal Processing by Gass et al., in Proceedings of the IEEE, v. 75, No. 9 (Sep. 1987) pp. 1246-125.
"Architecture and Design of the Mars Hardware Accelerator", Agra Wall, et. in 24.sup.th ACM/IEEE Design Automation Conference (1987), pp. 101-107.
"Digital Video & Image Processors", by O'Brien, Mather & Holland, published by Plessey Semiconductors (1989).
"An Architectureal Study, Design and Implementation of Digital Image Acquisition, Processing and Display Systems with Micro-Processor-Based Personal Computers and Charge-Coupled Device Imaging Technology", a dissertation by Robert J. Go SMU (1986).
"A Medium Grained Parallel Computer for Image Processing", by R.S. Cok, published by Digital Technology Center, Eastman Kodak Co., Rochester NY.

ART-UNIT: 273

PRIMARY-EXAMINER: Teska; Kevin J.

ASSISTANT-EXAMINER: Choi; Kyle J.

ATTY-AGENT-FIRM: Marshall, Jr.; Robert D. Brady, III; W. James Telecky, Jr.; Frederick J.

ABSTRACT:

There is disclosed a multi-processor system and method arranged, in one embodiment, as an image and graphics processor. The image processor is structured with several individual processors all having communication links to several memories. A crossbar switch serves to establish the processor memory links. The entire image processor, including the individual processors, the crossbar switch and the memories, is contained on a single silicon chip.

16 Claims, 64 Drawing figures

Previous Doc Next Doc Go to Doc#

L7: Entry 2 of 15 File: USPT May 30, 2000

DOCUMENT-IDENTIFIER: US 6070003 A
TITLE: System and method of memory access in apparatus having plural processors and plural memories

Abstract Text (1):
There is disclosed a multi-processor system and method arranged, in one embodiment, as an image and graphics processor. The image processor is structured with several individual processors all having communication links to several memories. A crossbar switch serves to establish the processor memory links. The entire image processor, including the individual processors, the crossbar switch and the memories, is contained on a single silicon chip.

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Detailed Description Text (134):
One of the reasons why so much imaging capability is available under the system shown is that the single chip contains several processors working in parallel together with several memories, all accessible under a crossbar switch which allows for substantially instantaneous rearrangement of the system. This gives a degree of power and flexibility not heretofore known. This then allows for a vast increase in the amount of imaging processing capability which can be utilized in conjunction with other processing capability to provide the type of services not known before. Some examples of this would be restoration of photographs and other images, or the cleaning of facsimile documents so that extraneous material in the background is removed yielding a received image as clear or clearer than the sending image. This entire system can be packaged in a relatively small package mainly because of the processing capability that is combined into one operational unit. Bandwidth limitations and other physical limitations such as wiring connections, are eliminated.

Current US Original Classification (1):
710/317

h e b b cg b cc e

L7: Entry 2 of 15 File: USPT May 30, 2000

US-PAT-NO: 6070003
DOCUMENT-IDENTIFIER: US 6070003 A

TITLE: System and method of memory access in apparatus having plural processors and plural memories

DATE-ISSUED: May 30, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gove; Robert J.	Plano	TX		
Balmer; Keith	Bedford			GB
Ing-Simmons; Nicholas Kerin	Bedford			GB
Guttag; Karl Marion	Missouri City	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 08/ 264582 [PALM]
DATE FILED: June 22, 1994

PARENT-CASE:
This application is a Continuation of application Ser. No. 07/437,852, filed Nov. 17, 1989 abandoned.

INT-CL: [07] G06 F 13/16

US-CL-ISSUED: 395/312
US-CL-CURRENT: 710/317

FIELD-OF-SEARCH: 395/200, 395/800

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4365292	December 1982	Barnes et al.	395/800
☐	4553203	November 1985	Rau et al.	395/800
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☐	4633245	December 1986	Blout et al.	340/825.03
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☐	4747043	May 1988	Rodman	364/200
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☐	4811201	March 1989	Rau et al.	395/325
☐	4930102	May 1990	Jennings	395/800
☐	4965718	October 1990	George et al.	395/800
☐	4985832	January 1991	Grondalski	395/800
☐	5020059	May 1991	Gonin et al.	395/800
☐	5041971	August 1991	Carvey et al.	395/800
☐	5056000	October 1991	Chang	395/800
☐	5083267	January 1992	Rau et al.	395/375
☐	5133073	July 1992	Jackson et al.	395/800
☐	5142686	August 1992	Hecht et al.	395/800

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OTHER PUBLICATIONS

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"The Androx Parallel Image Array Processor", by Wayne Threatt, in Electronic Imaging '87, International Electronic Imagining Exposition & Conference (1987), pp. 1061-1064.
"Real Time 3D Object Tracking in a Rapid Prototyping Environment", by Robert J. Gove in Electronic Imaging '88 (1988).
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"Handling Real Time Images Comes Naturally to Systolic Array Chip", by Hannaway, Shea Bishop, in Electronic Design, p. 289-300 (1984).
"Systolic Array Chip Recognizes Visual Patterns Quicker Than a Wink", by W.W. Smith, P. Sullivan, in Electronic Design, pp. 257-266 (1984).
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"High Resolution Frame Grabbing and Processing Through Parallel Architecture", by

Daniel Crevier published by Coreco, Inc., Quebec, Canada.
Multiple Digital Signal Processor Environment for Intelligent Signal Processing by Gass et al., in Proceedings of the IEEE, v. 75, No. 9 (Sep. 1987) pp. 1246-125.
"Architecture and Design of the Mars Hardware Accelerator", Agra Wall, et. in 24.sup.th ACM/IEEE Design Automation Conference (1987), pp. 101-107.
"Digital Video & Image Processors", by O'Brien, Mather & Holland, published by Plessey Semiconductors (1989).
"An Architectureal Study, Design and Implementation of Digital Image Acquisition, Processing and Display Systems with Micro-Processor-Based Personal Computers and Charge-Coupled Device Imaging Technology", a dissertation by Robert J. Go SMU (1986).
"A Medium Grained Parallel Computer for Image Processing", by R.S. Cok, published by Digital Technology Center, Eastman Kodak Co., Rochester NY.

ART-UNIT: 273

PRIMARY-EXAMINER: Teska; Kevin J.

ASSISTANT-EXAMINER: Choi; Kyle J.

ATTY-AGENT-FIRM: Marshall, Jr.; Robert D. Brady, III; W. James Telecky, Jr.; Frederick J.

ABSTRACT:

There is disclosed a multi-processor system and method arranged, in one embodiment, as an image and graphics processor. The image processor is structured with several individual processors all having communication links to several memories. A crossbar switch serves to establish the processor memory links. The entire image processor, including the individual processors, the crossbar switch and the memories, is contained on a single silicon chip.

16 Claims, 64 Drawing figures

Previous Doc Next Doc Go to Doc#

US-PAT-NO: 6667960

DOCUMENT-IDENTIFIER: US 6667960 B1

TITLE: Protocol for identifying components in a point-to-point computer system

First patent

---------- KWIC ---------

Abstract Text - ABTX (1):

A system and method of mapping a network topology in a network including a plurality of nodes which communicate over dedicated links which connect pairs of the nodes, where the method consists of the steps of exchanging respective network identification information between adjacent pairs of nodes, establishing communications with another of the nodes using the network identification information, obtaining network identification information of the other node from that node, using the network identification information to establish communications with other nodes, obtaining additional network identification information from those other nodes, repeating these steps until network identification information is obtained from all of the nodes of the network and using this information determine the network topology.

Brief Summary Text - BSTX (2):

Server class computer products are constructed by the combination of modular sets of computer components. These components can consist of a number of processors, a global-shared memory environment, main memory, PCI (Peripheral Components Interface) controllers and other components as required. Server class computer products can also be configured using basic building blocks. Example building blocks include a cell, a crossbar system, a routing chip and a PCI-based input/output (I/O) subsystem. In this case, a cell consists of shared multiprocessor (SMP) system containing from one to four (or more) processors, a portion of system memory and a connection to an I/O subsystem. Normally the cell is designed such that the hardware will not limit the mixture of different types of cells within the system. Cells can also be added or removed while the system is running. In typical systems, the cell resides on a single PC board.

US-PAT-NO: 6636949

DOCUMENT-IDENTIFIER: US 6636949 B2

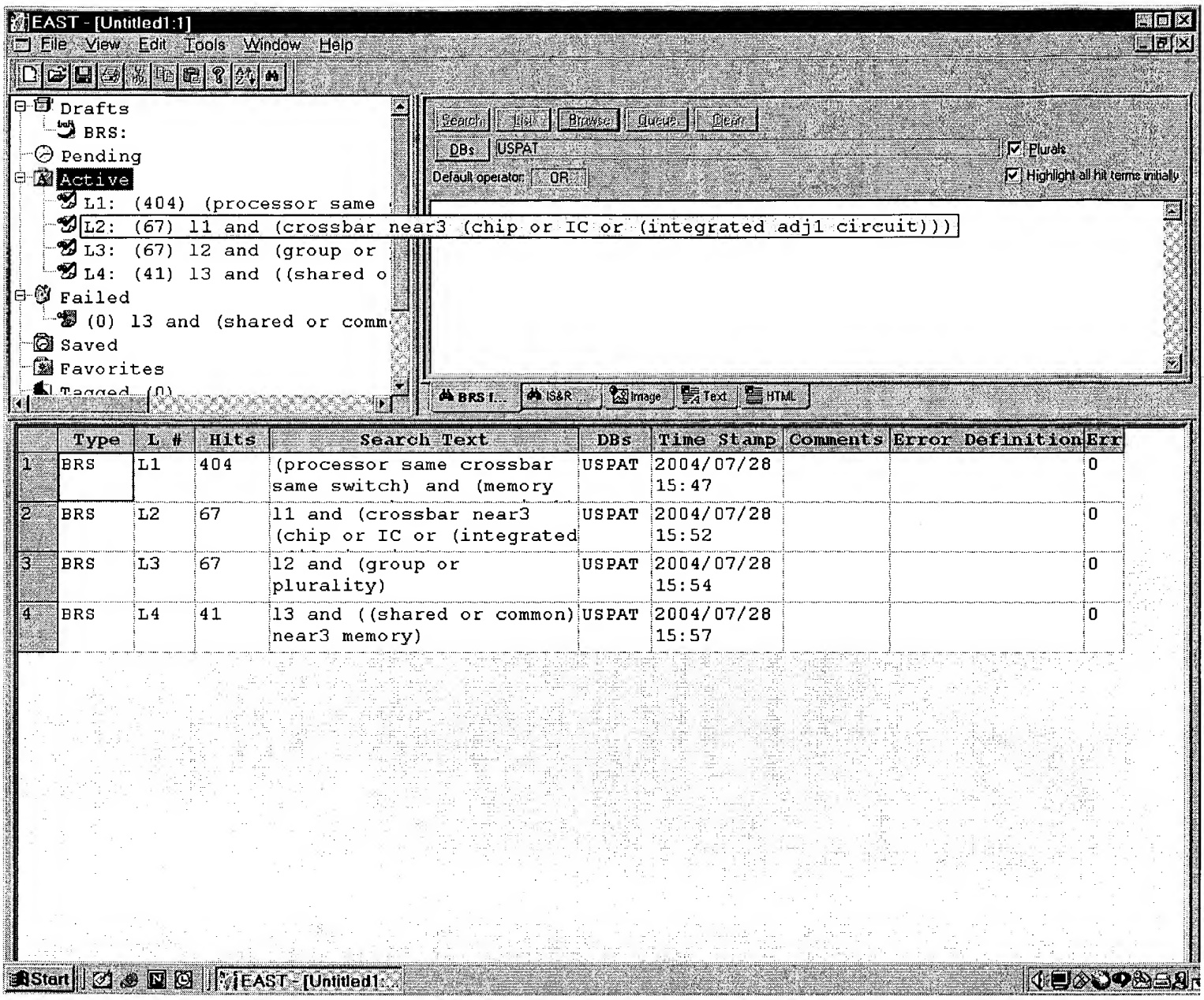
TITLE: System for handling coherence protocol races in a scalable shared memory system based on chip multiprocessing

---------- KWIC ---------

TITLE - TI (1):
System for handling coherence protocol races in a scalable shared memory system based on chip multiprocessing

Parent Case Text - PCTX (3):
This application is related to, and hereby incorporates by reference, the following U.S. patent applications: Multiprocessor Cache Coherence System And Method in Which Processor Nodes And Input/output Nodes Are Equal Participants, Ser. No. 09/878,984, filed Jun. 11, 2001; Scalable Multiprocessor System And Cache Coherence Method, Ser. No. 09/878,982, filed Jun. 11, 2001; System and Method for Daisy Chaining Cache Invalidation Requests in a Shared-memory Multiprocessor System, Ser. No. 09/878,985, filed Jun. 11, 2001; Cache Coherence Protocol Engine And Method For Processing Memory Transaction in Distinct Address Subsets During Interleaved Time Periods in a Multiprocessor System, Ser. No. 09/878,983, filed Jun. 11, 2001; System And Method For Generating Cache Coherence Directory Entries And Error Correction Codes in a Multiprocessor System, Ser. No. 09/972,477, filed Oct. 5, 2001, which claims priority on U.S. provisional patent application 60/238,330, filed Oct. 5, 2000, which is also hereby incorporated by reference in its entirety.

Brief Summary Text - BSTX (6):
This invention relates to the design of cache coherence protocol for a scalable shared memory system composed of chip multiprocessor nodes, that is, each processor chip contains multiple CPUs, each CPU with its own private instruction and data caches (first-level caches) and all CPUs sharing a single second-level cache. Cache coherence is maintained among all caches within a chip, as well among all caches across the nodes by a protocol engine and a



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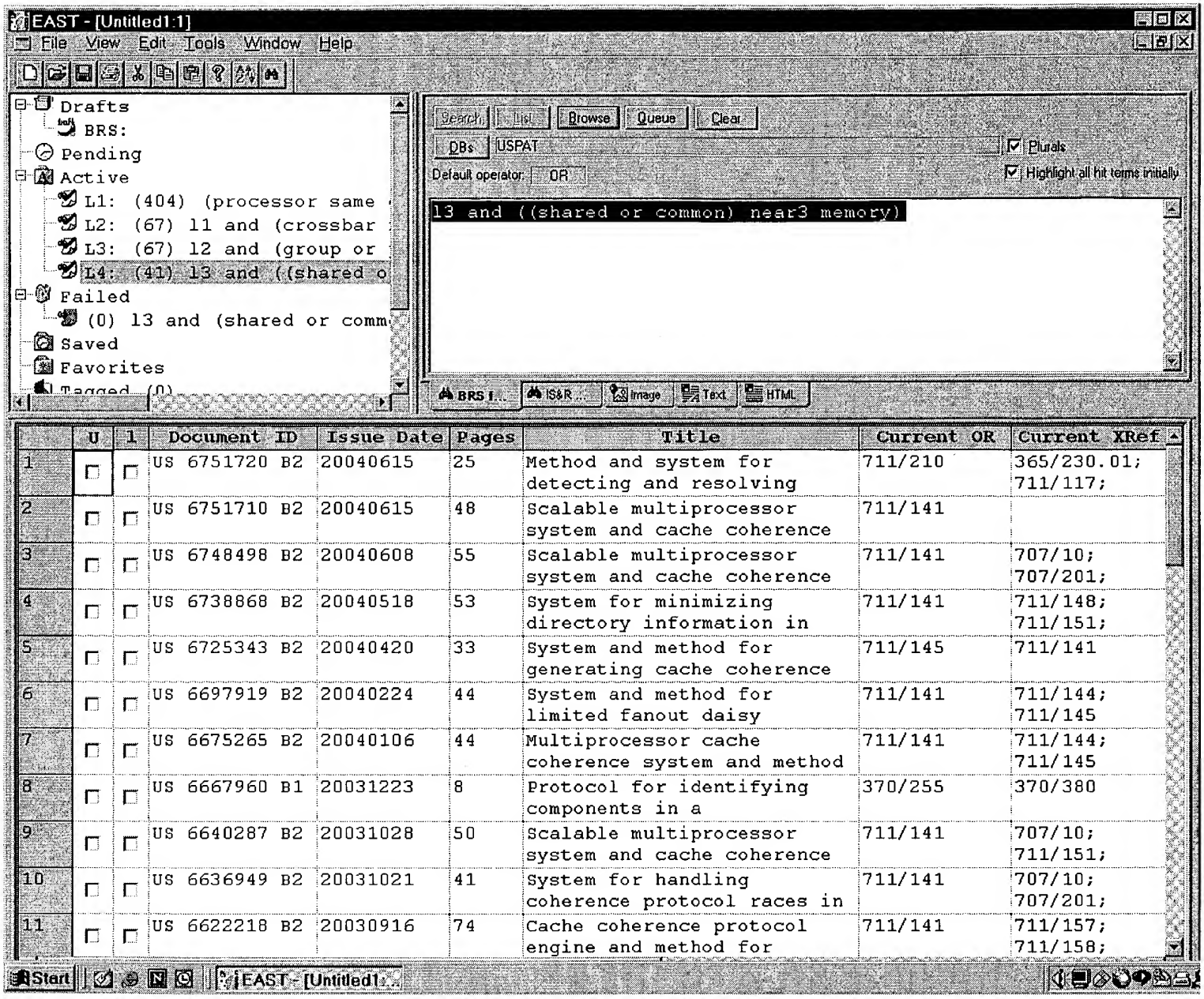
1	BRS	L1	404	(processor same crossbar same switch) and (memory	USPAT	2004/07/28 15:47			0
2	BRS	L2	67	l1 and (crossbar near3 (chip or IC or (integrated	USPAT	2004/07/28 15:52			0
3	BRS	L3	67	l2 and (group or plurality)	USPAT	2004/07/28 15:54			0
4	BRS	L4	41	l3 and ((shared or common) near3 memory)	USPAT	2004/07/28 15:57			0



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6751720 B2	20040615	25	Method and system for detecting and resolving	711/210	365/230.01; 711/117;
2	☐	☐	US 6751710 B2	20040615	48	Scalable multiprocessor system and cache coherence	711/141	
3	☐	☐	US 6748498 B2	20040608	55	Scalable multiprocessor system and cache coherence	711/141	707/10; 707/201;
4	☐	☐	US 6738868 B2	20040518	53	System for minimizing directory information in	711/141	711/148; 711/151;
5	☐	☐	US 6725343 B2	20040420	33	System and method for generating cache coherence	711/145	711/141
6	☐	☐	US 6697919 B2	20040224	44	System and method for limited fanout daisy	711/141	711/144; 711/145
7	☐	☐	US 6675265 B2	20040106	44	Multiprocessor cache coherence system and method	711/141	711/144; 711/145
8	☐	☐	US 6667960 B1	20031223	8	Protocol for identifying components in a	370/255	370/380
9	☐	☐	US 6640287 B2	20031028	50	Scalable multiprocessor system and cache coherence	711/141	707/10; 711/151;
10	☐	☐	US 6636949 B2	20031021	41	System for handling coherence protocol races in	711/141	707/10; 707/201;
11	☐	☐	US 6622218 B2	20030916	74	Cache coherence protocol engine and method for	711/141	711/157; 711/158;

Your search matched **2** of **1056955** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enter new one in the text box.

processor and memory and crossbar and switch and Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 **On crossbar switch and multiple bus interconnection networks with overlapping connectivity**
Wilkinson, B.;
Computers, IEEE Transactions on , Volume: 41 , Issue: 6 , June 1992
Pages:738 - 746

[Abstract] [PDF Full-Text (804 KB)] **IEEE JNL**

2 **Cost-performance analysis of cascaded crossbar interconnected multiprocessors**
Evequoz, C.;
Computers and Digital Techniques, IEE Proceedings- , Volume: 142 , Issue: 2 , March 1995
Pages:117 - 134

[Abstract] [PDF Full-Text (908 KB)] **IEE JNL**

On crossbar switch and multiple bus interconnectio networks with overlapping connectivity

Wilkinson, B.
Dept. of Comput. Sci., North Carolina Univ., Charlotte, NC, USA;
This paper appears in: **Computers, IEEE Transactions on**

Publication Date: June 1992
On page(s): 738 - 746
Volume: 41 , Issue: 6
ISSN: 0018-9340
Reference Cited: 11
CODEN: ITCOB4
Inspec Accession Number: 4226493

Abstract:
Multiprocessor interconnection networks are proposed which have the charact each **processor** or **memory** module can connect to a **group** of its near neigh adjacent directly connected **groups** include some of the same **processors** or **memories**. These overlapping connectivity networks are attractive especially large number of **processors** which cannot be provided with full connectivity t operate by communication between **processors**. Applications for overlapping connectivity networks include neural computers and dataflow computers. Ban formulas are derived using a probabilistic approach, including when intermedi **processors** are used in the interconnection path. A general cell design is pre capable of representing various overlapping connectivity networks

Index Terms:
multiprocessor interconnection networks dataflow computers multiple bus interconnec networks neural computers overlapping connectivity overlapping connectivity networ

Documents that cite this document
There are no citing documents available in IEEE Xplore at this time.

Search Results [PDF FULL-TEXT 804 KB] NEXT DOWNLOAD CITATION

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Cost-performance analysis of cascaded crossbar interconnected multiprocessors

Evequoz, C.
DGEGI Section Informatique, Ecole Polytech., Montreal, Que.

This paper appears in: **Computers and Digital Techniques, IEE Proceedir**

Publication Date: March 1995
On page(s): 117 - 134
Volume: 142 , Issue: 2
ISSN: 1350-2387
Reference Cited: 10
CODEN: ICDTEA
Inspec Accession Number: 4924402

Abstract:
The cost performance ratio of interconnection networks for multiprocessors de the connectivity of the network: the processing efficiency of these systems in when the number of links and **switches** also increases. The authors study the performance of a class of interconnection networks in which **processors** and modules are **grouped** into stages, each consisting of a **crossbar** network. Ea connected to two neighbouring stages. A queueing model is presented to anal cascaded **crossbar** architectures organised into bidirectional rings and operat synchronous packet **switching**. Cost performance comparisons of various cas **crossbar** network configurations are presented. It is shown that, even with p **memory** reference locality, it is preferable to have more stages and fewer **pr** per stage

Index Terms:
cascade networks multiprocessor interconnection networks packet **switching** perfor evaluation queueing theory bidirectional rings cascaded **crossbar** architectures cas **crossbar** interconnected multiprocessors connectivity cost performance ratio **crossb** interconnection networks **memory** modules processing efficiency queueing model packet **switching**

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